32 Mbit (x8/x16) Concurrent SuperFlash

SST36VF3203 / SST36VF3204

Advance Information

FEATURES:

- **Organized as 2M x16 or 4M x8**
- **Dual Bank Architecture for Concurrent Read/Write Operation**
  - 32 Mbit Bottom Sector Protection (in the smaller bank)
    - SST36VF3203: 24 Mbit + 8 Mbit
  - 32 Mbit Top Sector Protection (in the smaller bank)
    - SST36VF3204: 8 Mbit + 24 Mbit
- **Single 2.7-3.6V for Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 6 mA typical
  - Standby Current: 4 µA typical
  - Auto Low Power Mode: 4 µA typical
- **Hardware Sector Protection/WP# Input Pin**
  - Protects 8 KWord in the smaller bank or, top or bottom bank for 16 Mbit+16 Mbit, by driving WP# low and unprotects by driving WP# high
- **Hardware Reset Pin (RST#)**
  - Resets the internal state machine to reading array data
- **Byte# Pin**
  - Selects 8-bit or 16-bit mode
- **Sector-Erase Capability**
  - Uniform 2 KWord sectors
- **Chip-Erase Capability**
- **Block-Erase Capability**
  - Uniform 32 KWord blocks
- **Erase-Suspend / Erase-Resume Capabilities**
- **Security ID Feature**
  - SST: 128 bits
  - User: 256 Bytes
- **Fast Read Access Time**
  - 70 ns
- **Latched Address and Data**
- **Fast Erase and Program (typical):**
  - Sector-Erase Time: 18 ms
  - Block-Erase Time: 18 ms
  - Chip-Erase Time: 35 ms
  - Program Time: 7 µs
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
  - Ready/Busy# pin
- **CMOS I/O Compatibility**
- **Conforms to Common Flash Memory Interface (CFI)**
- **JEDEC Standards**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 48-ball TFBGA (6mm x 8mm)
  - 48-lead TSOP (12mm x 20mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST36VF320x are 2M x16 or 4M x8 CMOS Concurrent Read/Write Flash Memory manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The devices write (Program or Erase) with a 2.7-3.6V power supply and conform to JEDEC standard pinouts for x8/x16 memories.

Featuring high performance Word-Program, these devices provide a typical Program time of 7 µsec and use the Toggle Bit, Data# Polling, or RY/BY# to detect the completion of the Program or Erase operation. To protect against inadvertent write, the devices have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

These devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the devices significantly improve performance and reliability, while lowering power consumption. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

Advance Information

SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high-density, surface-mount requirements, these devices are offered in 48-ball TFBGA and 48-lead TSOP packages. See Figures 1 and 2 for pin assignments.

Device Operation

Memory operation functions are initiated using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Auto Low Power Mode

These devices also have the **Auto Lower Power** mode which puts them in a near standby mode within 500 ns after data has been accessed with a valid Read operation. This reduces the I_{DD} active Read current to 4 µA typically. While CE# is low, the devices exit Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty.

Concurrent Read/Write Operation

The dual bank architecture of these devices allows the Concurrent Read/Write operation whereby the user can read from one bank while programming or erasing in the other bank. For example, reading system code in one bank while updating data in the other bank.

CONCURRENT READ/WRITE STATE

Bank 1	Bank 2
Read	No Operation
Read	Write
Write	Read
Write	No Operation
No Operation	Read
No Operation	Write

Note: For the purposes of this table, write means to perform Block- or Sector-Erase or Program operations as applicable to the appropriate bank.

Read Operation

The Read operation is controlled by CE# and OE#; both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in a high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 3).

Program Operation

These devices are programmed on a word-by-word or byte-by-byte basis depending on the state of the BYTE# pin. Before programming, one must ensure that the sector which is being programmed is fully erased.

The Program operation is accomplished in three steps:

1. Software Data Protection is initiated using the three-byte load sequence.
2. Address and data are loaded.

   During the Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first.
3. The internal Program operation is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed typically within 7 µs.

See Figures 4 and 5 for WE# and CE# controlled Program operation timing diagrams and Figure 19 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during an internal Program operation are ignored.

Sector- (Block-) Erase Operation

These devices offer both Sector-Erase and Block-Erase operations. These operations allow the system to erase the devices on a sector-by-sector (or block-by-block) basis. The sector architecture is based on a uniform sector size of 2 KWord. The Block-Erase mode is based on a uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with a Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. Any commands issued during the Sector- or Block-Erase operation are ignored except Erase-Suspend and Erase-Resume. See Figures 9 and 10 for timing waveforms.

Chip-Erase Operation

The devices provide a Chip-Erase operation, which allows the user to erase all sectors/blocks to the “1” state. This is useful when a device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid Read is Toggle Bit or Data# Polling. Any commands issued during the Chip-Erase operation are ignored. See Table 7 for the command sequence, Figure 8 for timing diagram, and Figure 22 for the flowchart. When WP# is low, any attempt to Chip-Erase will be ignored.

Erase-Suspend/Erase-Resume Operations

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location, or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing a one-byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode within 20 µs after the Erase-Suspend command had been issued. Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ_2 toggling and DQ_6 at “1”. While in Erase-Suspend mode, a Program operation is allowed except for the sector or block selected for Erase-Suspend. The Software ID Entry command can also be executed. To resume Sector-Erase or Block-Erase operation which has been suspended, the system must issue an Erase-Resume command. The operation is executed by issuing a one-byte command sequence with Erase Resume command (30H) at any address in the last byte sequence.

Write Operation Status Detection

These devices provide one hardware and two software means to detect the completion of a Write (Program or Erase) cycle in order to optimize the system Write cycle time. The hardware detection uses the Ready/Busy# (RY/BY#) output pin. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Ready/Busy# (RY/BY#), a Data# Polling (DQ_7), or Toggle Bit (DQ_6) Read may be simultaneous with the completion of the Write cycle. If this occurs, the system may get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both Reads are valid, then the Write cycle has completed, otherwise the rejection is valid.

Ready/Busy# (RY/BY#)

The devices include a Ready/Busy# (RY/BY#) output signal. RY/BY# is an open drain output pin that indicates whether an Erase or Program operation is in progress. Since RY/BY# is an open drain output, it allows several devices to be tied in parallel to V_{DD} via an external pull-up resistor. After the rising edge of the final WE# pulse in the command sequence, the RY/BY# status is valid.

When RY/BY# is actively pulled low, it indicates that an Erase or Program operation is in progress. When RY/BY# is high (Ready), the devices may be read or left in standby mode.

Byte/Word (BYTE#)

The device includes a BYTE# pin to control whether the device data I/O pins operate x8 or x16. If the BYTE# pin is at logic "1" (V_{IH}) the device is in x16 data configuration: all data I/0 pins DQ_0-DQ_{15} are active and controlled by CE# and OE#.

If the BYTE# pin is at logic "0", the device is in x8 data configuration: only data I/O pins DQ_0-DQ_7 are active and controlled by CE# and OE#. The remaining data pins DQ_8-DQ_{14} are at Hi-Z, while pin DQ_{15} is used as the address input A_{-1} for the Least Significant Bit of the address bus.

Data# Polling (DQ_7)

When the devices are in an internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 6 for Data# Polling (DQ_7) timing diagram and Figure 20 for a flowchart.

Toggle Bits (DQ_6 and DQ_2)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating "1"s and "0"s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ_6 bit will stop toggling. The device is then ready for the next operation. The toggle bit is valid after the rising edge of the fourth WE# (or CE#) pulse for Program operations. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ_6) is valid after the rising edge of sixth WE# (or CE#) pulse. DQ_6 will be set to "1" if a Read operation is attempted on an Erase-suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ_6 will toggle.

An additional Toggle Bit is available on DQ_2, which can be used in conjunction with DQ_6 to check whether a particular sector is being actively erased or erase-suspended. Table 1 shows detailed status bit information. The Toggle Bit (DQ_2) is valid after the rising edge of the last WE# (or CE#) pulse of a Write operation. See Figure 7 for Toggle Bit timing diagram and Figure 20 for a flowchart.

TABLE 1: WRITE OPERATION STATUS

Status		DQ_7	DQ_6	DQ_2	RY/BY#
Normal Operation	Standard Program	DQ7#	Toggle	No Toggle	0
	Standard Erase	0	Toggle	Toggle	0
Erase-Suspend Mode	Read From Erase Suspended Sector/Block	1	1	Toggle	1
	Read From Non-Erase Suspended Sector/Block	Data	Data	Data	1
	Program	DQ7#	Toggle	N/A	0

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Note: DQ_7, DQ_6, and DQ_2 require a valid address when reading status information. The address must be in the bank where the operation is in progress in order to read the operation status. If the address is pointing to a different bank (not busy), the device will output array data.

Data Protection

The devices provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The devices provide hardware block protection which protects the outermost 8 KWord in the smaller bank or, top or bottom bank for 16 Mbit +16 Mbit. The block is protected when WP# is held low. When WP# is held low and a Block-Erase command is issued to the protected black, the data in the outermost 8 KWord/16 KByte section will be protected. The rest of the block will be erased. See Tables 3 and 4 for Block-Protection location.

A user can disable block protection by driving WP# high. This allows data to be erased or programmed into the protected sectors. WP# must be held high prior to issuing the Write command and remain stable until after the entire Write operation has completed. If WP# is left floating, it is internally held high via a pull-up resistor, and the Boot Block is unprotected, enabling Program and Erase operations on that block.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the devices to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see Figure 16) and all output pins are set to High-Z. When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 15).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

These devices provide the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of the six-byte sequence. The devices are shipped with the Software Data Protection permanently enabled. See Table 7 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value during any SDP command sequence.

Common Flash Memory Interface (CFI)

These devices also contain the CFI information to describe the characteristics of the devices. In order to enter the CFI Query mode, the system must write the three-byte sequence, same as the Software ID Entry command with 98H (CFI Query command) to address BK_X555H in the last byte sequence. In order to enter the CFI Query mode, the system can also use the one-byte sequence with BK_X55H on Address and 98H on Data Bus. See Figure 12 for CFI Entry and Read timing diagram. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 8 through 10. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

Security ID

The SST36VF320x devices offer a 136-word Security ID space. The Secure ID space is divided into two segments—one 128-bit factory programmed segment and one 128-word (256-byte) user-programmed segment. The first segment is programmed and locked at SST with a unique, 128-bit number. The user segment is left un-programmed for the customer to program as desired. To program the user segment of the Security ID, the user must use the Security ID Program command. End-of-Write status is checked by reading the toggle bits. Data# Polling is not used for Security ID End-of-Write detection. Once programming is complete, the Sec ID should be locked using the User Sec ID Program Lock-Out. This disables any future corruption of this space. Note that regardless of whether or not the Sec ID is locked, neither Sec ID segment can be erased. The Secure ID space can be queried by executing a three-byte command sequence with Query Sec ID command (88H) at address 555H in the last byte sequence. See Figure 14 for timing diagram. To exit this mode, the Exit Sec ID command should be executed. Refer to Table 7 for more details.

Product Identification

The Product Identification mode identifies the devices and manufacturer. For details, see Table 2 for software operation, Figure 11 for the Software ID Entry and Read timing diagram and Figure 21 for the Software ID Entry command sequence flowchart. The addresses A_{20} and A_{18} indicate a bank address. When the addressed bank is switched to Product Identification mode, it is possible to read another address from the same bank without issuing a new Software ID Entry command. The Software ID Entry command may be written to an address within a bank that is in Read Mode or in Erase-Suspend mode. The Software ID Entry command may not be written while the device is programming or erasing in the other bank.

TABLE 2: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	BK_X0000H	00BFH
Device ID		
SST36VF3203	BK_X0001H	7354H
SST36VF3204	BK_X0001H	7353H

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Note: BK_X = Bank Address (A_{20}-A_{18})

Product Identification Mode Exit/CFI Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 7 for the software command code, Figure 13 for timing waveform and Figure 21 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM

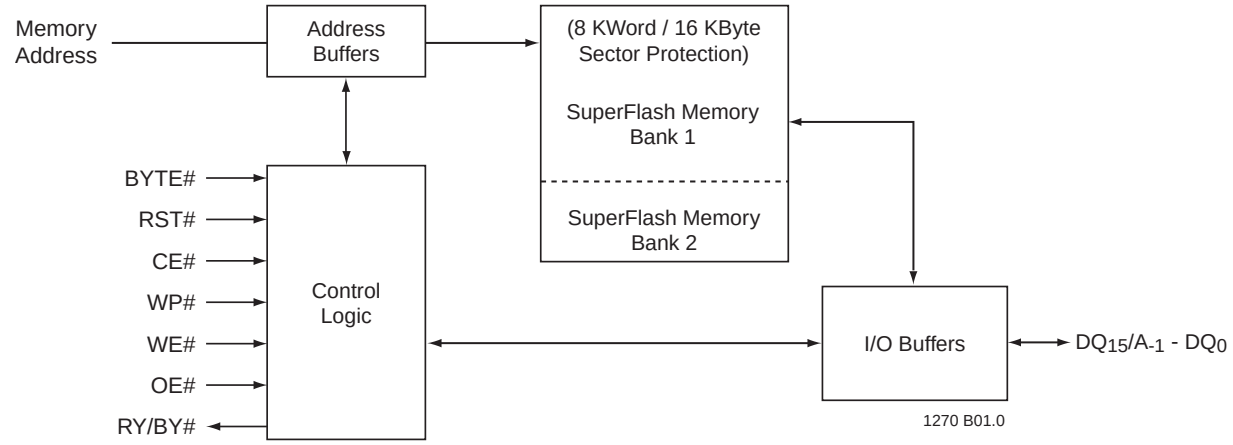

TABLE 3: SST36VF3203, 2M x16 CSF BOTTOM DUAL-BANK MEMORY ORGANIZATION (1 OF 2)

SST36VF3203	Block	Block Size	Address Range x8	Address Range x16
Bank 1	BA0	8 KW / 16 KB	000000H–003FFFH	000000H–001FFFH
		24 KW / 48 KB	004000H–00FFFFH	002000H–007FFFH
	BA1	32 KW / 64 KB	010000H–01FFFFH	008000H–00FFFFH
	BA2	32 KW / 64 KB	020000H–02FFFFH	010000H–017FFFH
	BA3	32 KW / 64 KB	030000H–03FFFFH	018000H–01FFFFH
	BA4	32 KW / 64 KB	040000H–04FFFFH	020000H–027FFFH
	BA5	32 KW / 64 KB	050000H–05FFFFH	028000H–02FFFFH
	BA6	32 KW / 64 KB	060000H—06FFFFH	030000H–037FFFH
	BA7	32 KW / 64 KB	070000H—07FFFFH	038000H–03FFFFH
	BA8	32 KW / 64 KB	080000H—08FFFFH	040000H–047FFFH
	BA9	32 KW / 64 KB	090000H—09FFFFH	048000H–04FFFFH
	BA10	32 KW / 64 KB	0A0000H—0AFFFFH	050000H–057FFFH
	BA11	32 KW / 64 KB	0B0000H—0BFFFFH	058000H–05FFFFH
	BA12	32 KW / 64 KB	0C0000H—0CFFFFH	060000H–067FFFH
	BA13	32 KW / 64 KB	0D0000H—0DFFFFH	068000H–06FFFFH
	BA14	32 KW / 64 KB	0E0000H—0EFFFFH	070000H–077FFFH
	BA15	32 KW / 64 KB	0F0000H—0FFFFFH	078000H–07FFFFH
Bank 2	BA16	32 KW / 64 KB	100000H—10FFFFH	080000H–087FFFH
	BA17	32 KW / 64 KB	110000H—11FFFFH	088000H–08FFFFH
	BA18	32 KW / 64 KB	120000H—12FFFFH	090000H–097FFFH
	BA19	32 KW / 64 KB	130000H—13FFFFH	098000H–09FFFFH
	BA20	32 KW / 64 KB	140000H—14FFFFH	0A0000H–0A7FFFH
	BA21	32 KW / 64 KB	150000H—15FFFFH	0A8000H–0AFFFFH
	BA22	32 KW / 64 KB	160000H—16FFFFH	0B0000H–0B7FFFH
	BA23	32 KW / 64 KB	170000H—17FFFFH	0B8000H–0BFFFFH
	BA24	32 KW / 64 KB	180000H—18FFFFH	0C0000H–0C7FFFH
	BA25	32 KW / 64 KB	190000H—19FFFFH	0C8000H–0CFFFFH
	BA26	32 KW / 64 KB	1A0000H—1AFFFFH	0D0000H–0D7FFFH
	BA27	32 KW / 64 KB	1B0000H—1BFFFFH	0D8000H–0DFFFFH
	BA28	32 KW / 64 KB	1C0000H—1CFFFFH	0E0000H—0E7FFFH
	BA29	32 KW / 64 KB	1D0000H—1DFFFFH	0E8000H—0EFFFFH
	BA30	32 KW / 64 KB	1E0000H—1EFFFFH	0F0000H—0F7FFFH
	BA31	32 KW / 64 KB	1F0000H—1FFFFFH	0F8000H—0FFFFFH
	BA32	32 KW / 64 KB	200000H—20FFFFH	100000H—107FFFH
	BA33	32 KW / 64 KB	210000H—21FFFFH	108000H—10FFFFH
	BA34	32 KW / 64 KB	220000H—22FFFFH	110000H—117FFFH
	BA35	32 KW / 64 KB	230000H—23FFFFH	118000H—11FFFFH
	BA36	32 KW / 64 KB	240000H—24FFFFH	120000H—127FFFH
	BA37	32 KW / 64 KB	250000H—25FFFFH	128000H—12FFFFH
	BA38	32 KW / 64 KB	260000H—26FFFFH	130000H—137FFFH
	BA39	32 KW / 64 KB	270000H—27FFFFH	138000H—13FFFFH
	BA40	32 KW / 64 KB	280000H—28FFFFH	140000H—147FFFH
	BA41	32 KW / 64 KB	290000H—29FFFFH	148000H—14FFFFH

TABLE 3: SST36VF3203, 2M x16 CSF BOTTOM DUAL-BANK MEMORY ORGANIZATION (CONTINUED) (2 OF 2)

SST36VF3203	Block	Block Size	Address Range x8	Address Range x16
Bank 2	BA42	32 KW / 64 KB	2A0000H—2AFFFFH	150000H—157FFFH
	BA43	32 KW / 64 KB	2B0000H–2BFFFFH	158000H–15FFFFH
	BA44	32 KW / 64 KB	2C0000H–2CFFFFH	160000H–167FFFH
	BA45	32 KW / 64 KB	2D0000H–2DFFFFH	168000H–16FFFFH
	BA46	32 KW / 64 KB	2E0000H–2EFFFFH	170000H–177FFFH
	BA47	32 KW / 64 KB	2F0000H–2FFFFFH	178000H–17FFFFH
	BA48	32 KW / 64 KB	300000H–30FFFFH	180000H–187FFFH
	BA49	32 KW / 64 KB	310000H–31FFFFH	188000H–18FFFFH
	BA50	32 KW / 64 KB	320000H–32FFFFH	190000H–197FFFH
	BA51	32 KW / 64 KB	330000H–33FFFFH	198000H–19FFFFH
	BA52	32 KW / 64 KB	340000H–34FFFFH	1A0000H–1A7FFFH
	BA53	32 KW / 64 KB	350000H–35FFFFH	1A8000H–1AFFFFH
	BA54	32 KW / 64 KB	360000H–36FFFFH	1B0000H–1B7FFFH
	BA55	32 KW / 64 KB	370000H–37FFFFH	1B8000H–1BFFFFH
	BA56	32 KW / 64 KB	380000H–38FFFFH	1C0000H–1C7FFFH
	BA57	32 KW / 64 KB	390000H–39FFFFH	1C8000H–1CFFFFH
	BA58	32 KW / 64 KB	3A0000H–3AFFFFH	1D0000H–1D7FFFH
	BA59	32 KW / 64 KB	3B0000H–3BFFFFH	1D8000H–1DFFFFH
	BA60	32 KW / 64 KB	3C0000H–3CFFFFH	1E0000H–1E7FFFH
	BA61	32 KW / 64 KB	3D0000H–3DFFFFH	1E8000H–1EFFFFH
	BA62	32 KW / 64 KB	3E0000H–3EFFFFH	1F0000H–1F7FFFH
	BA63	32 KW / 64 KB	3F0000H–3FFFFFH	1F8000H–1FFFFFH

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TABLE 4: SST36VF3204, 2M x16 CSF Top Dual-Bank Memory Organization (1 of 2)

SST36VF3204	Block	Block Size	Address Range x8	Address Range x16
Bank 2	BA0	32 KW / 64 KB	000000H–00FFFFH	000000H–007FFFH
	BA1	32 KW / 64 KB	010000H–01FFFFH	008000H–00FFFFH
	BA2	32 KW / 64 KB	020000H–02FFFFH	010000H–017FFFH
	BA3	32 KW / 64 KB	030000H–03FFFFH	018000H–01FFFFH
	BA4	32 KW / 64 KB	040000H–04FFFFH	020000H–027FFFH
	BA5	32 KW / 64 KB	050000H–05FFFFH	028000H–02FFFFH
	BA6	32 KW / 64 KB	060000H—06FFFFH	030000H–037FFFH
	BA7	32 KW / 64 KB	070000H—07FFFFH	038000H–03FFFFH
	BA8	32 KW / 64 KB	080000H—08FFFFH	040000H–047FFFH
	BA9	32 KW / 64 KB	090000H—09FFFFH	048000H–04FFFFH
	BA10	32 KW / 64 KB	0A0000H—0AFFFFH	050000H–057FFFH
	BA11	32 KW / 64 KB	0B0000H—0BFFFFH	058000H–05FFFFH
	BA12	32 KW / 64 KB	0C0000H—0CFFFFH	060000H–067FFFH
	BA13	32 KW / 64 KB	0D0000H—0DFFFFH	068000H–06FFFFH
	BA14	32 KW / 64 KB	0E0000H—0EFFFFH	070000H–077FFFH
	BA15	32 KW / 64 KB	0F0000H—0FFFFFH	078000H–07FFFFH
	BA16	32 KW / 64 KB	100000H—10FFFFH	080000H–087FFFH
	BA17	32 KW / 64 KB	110000H—11FFFFH	088000H–08FFFFH
	BA18	32 KW / 64 KB	120000H—12FFFFH	090000H–097FFFH
	BA19	32 KW / 64 KB	130000H—13FFFFH	098000H–09FFFFH
	BA20	32 KW / 64 KB	140000H—14FFFFH	0A0000H–0A7FFFH
	BA21	32 KW / 64 KB	150000H—15FFFFH	0A8000H–0AFFFFH
	BA22	32 KW / 64 KB	160000H—16FFFFH	0B0000H–0B7FFFH
	BA23	32 KW / 64 KB	170000H—17FFFFH	0B8000H–0BFFFFH
	BA24	32 KW / 64 KB	180000H—18FFFFH	0C0000H–0C7FFFH
	BA25	32 KW / 64 KB	190000H—19FFFFH	0C8000H–0CFFFFH
	BA26	32 KW / 64 KB	1A0000H—1AFFFFH	0D0000H–0D7FFFH
	BA27	32 KW / 64 KB	1B0000H—1BFFFFH	0D8000H–0DFFFFH
	BA28	32 KW / 64 KB	1C0000H—1CFFFFH	0E0000H–0E7FFFH
	BA29	32 KW / 64 KB	1D0000H—1DFFFFH	0E8000H–0EFFFFH
	BA30	32 KW / 64 KB	1E0000H—1EFFFFH	0F0000H–0F7FFFH
	BA31	32 KW / 64 KB	1F0000H—1FFFFFH	0F8000H–0FFFFFH
	BA32	32 KW / 64 KB	200000H—20FFFFH	100000H–107FFFH
	BA33	32 KW / 64 KB	210000H—21FFFFH	108000H–10FFFFH
	BA34	32 KW / 64 KB	220000H—22FFFFH	110000H–117FFFH
	BA35	32 KW / 64 KB	230000H—23FFFFH	118000H–11FFFFH
	BA36	32 KW / 64 KB	240000H—24FFFFH	120000H–127FFFH
	BA37	32 KW / 64 KB	250000H—25FFFFH	128000H–12FFFFH
	BA38	32 KW / 64 KB	260000H—26FFFFH	130000H–137FFFH
	BA39	32 KW / 64 KB	270000H—27FFFFH	138000H–13FFFFH
	BA40	32 KW / 64 KB	280000H—28FFFFH	140000H–147FFFH
	BA41	32 KW / 64 KB	290000H—29FFFFH	148000H–14FFFFH
	BA42	32 KW / 64 KB	2A0000H—2AFFFFH	150000H–157FFFH

Advance Information

TABLE 4: SST36VF3204, 2M x16 CSF Top Dual-Bank Memory Organization (Continued) (2 of 2)

SST36VF3204	Block	Block Size	Address Range x8	Address Range x16
Bank 2	BA43	32 KW / 64 KB	2B0000H–2BFFFFH	158000H–15FFFFH
	BA44	32 KW / 64 KB	2C0000H–2CFFFFH	160000H–167FFFH
	BA45	32 KW / 64 KB	2D0000H–2DFFFFH	168000H–16FFFFH
	BA46	32 KW / 64 KB	2E0000H–2EFFFFH	170000H–177FFFH
	BA47	32 KW / 64 KB	2F0000H–2FFFFFH	178000H–17FFFFH
Bank 1	BA48	32 KW / 64 KB	300000H–30FFFFH	180000H–187FFFH
	BA49	32 KW / 64 KB	310000H–31FFFFH	188000H–18FFFFH
	BA50	32 KW / 64 KB	320000H–32FFFFH	190000H–197FFFH
	BA51	32 KW / 64 KB	330000H–33FFFFH	198000H–19FFFFH
	BA52	32 KW / 64 KB	340000H–34FFFFH	1A0000H–1A7FFFH
	BA53	32 KW / 64 KB	350000H–35FFFFH	1A8000H–1AFFFFH
	BA54	32 KW / 64 KB	360000H–36FFFFH	1B0000H–1B7FFFH
	BA55	32 KW / 64 KB	370000H–37FFFFH	1B8000H–1BFFFFH
	BA56	32 KW / 64 KB	380000H–38FFFFH	1C0000H–1C7FFFH
	BA57	32 KW / 64 KB	390000H–39FFFFH	1C8000H–1CFFFFH
	BA58	32 KW / 64 KB	3A0000H–3AFFFFH	1D0000H–1D7FFFH
	BA59	32 KW / 64 KB	3B0000H–3BFFFFH	1D8000H–1DFFFFH
	BA60	32 KW / 64 KB	3C0000H–3CFFFFH	1E0000H–1E7FFFH
	BA61	32 KW / 64 KB	3D0000H–3DFFFFH	1E8000H–1EFFFFH
	BA62	32 KW / 64 KB	3E0000H–3EFFFFH	1F0000H–1F7FFFH
	BA63	24 KW / 48 KB	3F0000H–3FBFFFH	1F8000H–1FDFFFH
		8 KW / 16 KB	3FC000H–3FFFFFH	1FE000H–1FFFFFH

T4.0 1270

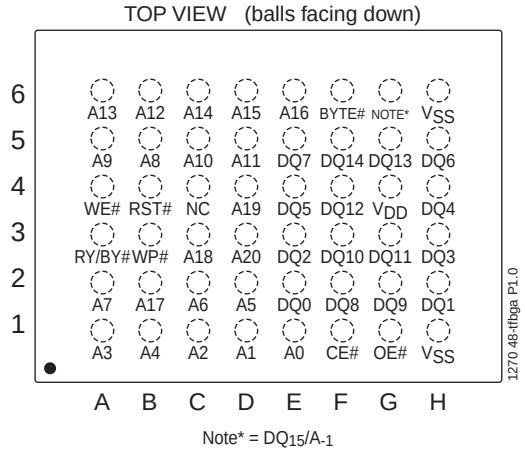


FIGURE 1: PIN ASSIGNMENTS FOR 48-BALL TFBGA (6MM X 8MM)

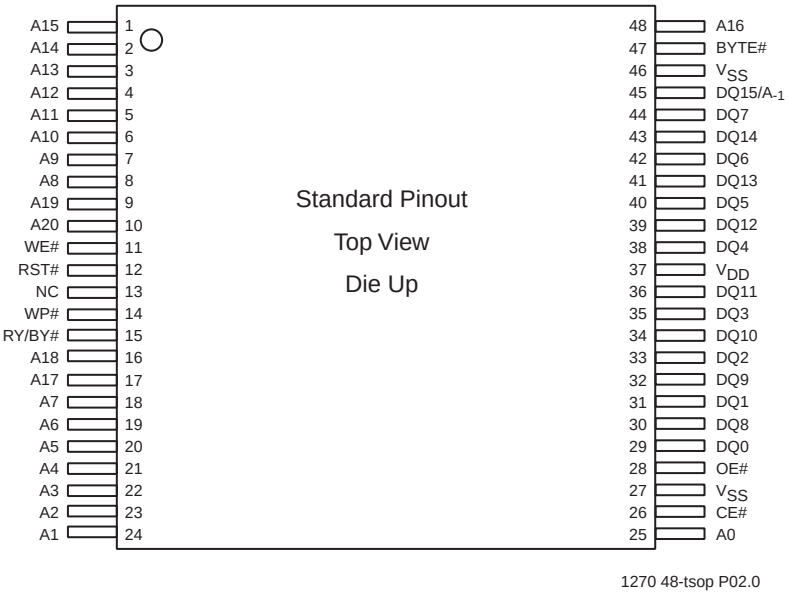


FIGURE 2: PIN ASSIGNMENTS FOR 48-LEAD TSOP (12MM X 20MM)

TABLE 5: PIN DESCRIPTION

Symbol	Name	Functions
A_{20}-A_0	Address Inputs	To provide memory addresses. During Sector-Erase and Hardware Sector Protection, A_{20}-A_{11} address lines will select the sector. During Block-Erase A_{20}-A_{15} address lines will select the block.
DQ_{14}-DQ_0	Data Input/Output	To output data during Read cycles and receive input data during Write cycles Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
DQ_{15}/A_{-1}	Data Input/Output and LBS Address	DQ_{15} is used as data I/O pin when in x16 mode (BYTE# = "1") A_{-1} is used as the LSB address pin when in x8 mode (BYTE# = "0")
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable	To control the Write operations
RST#	Hardware Reset	To reset and return the device to Read mode
RY/BY#	Ready/Busy#	To output the status of a Program or Erase operation RY/BY# is a open drain output, so a 10KΩ - 100KΩ pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read.
WP#	Write Protect	To protect and unprotect top or bottom 8 KWord (4 outermost sectors) from Erase or Program operation.
BYTE#	Word/Byte Configuration	To select 8-bit or 16-bit mode.
V_{DD}	Power Supply	To provide 2.7-3.6V power supply voltage
V_{SS}	Ground	
NC	No Connection	Unconnected pins

T5.0 1270

TABLE 6: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	RST#	DQ_7-DQ_0	DQ_{15}-DQ_8		Address
						BYTE# = V_{IH}	BYTE# = V_{IL}	
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	D_{OUT}	D_{OUT}	DQ_{14}-DQ_8 = High Z	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{IN}	D_{IN}	DQ_{15} = A_{-1}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[1]	X	High Z	Sector or Block address, 555H for Chip-Erase
Standby	V_{IHC}	X	X	V_{IHC}	High Z	High Z	High Z	X
Write Inhibit	X	V_{IL}	X	V_{IH}	High Z / D_{OUT}	High Z / D_{OUT}	High Z	X
	X	X	V_{IH}	V_{IH}	High Z / D_{OUT}	High Z / D_{OUT}	High Z	X
Product Identification								
Software Mode	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Manufacturer's ID (BFH)	Manufacturer's ID (00H)	High Z	See Table 7
					Device ID[2]	Device ID[2]	High Z	
Reset	X	X	X	V_{IL}	High Z	High Z	High Z	X

T6.1 1270

1. X can be V_{IL} or V_{IH}, but no other value.
2. Device ID = SST36VF3203 = 7354H, SST36VF3204 = 7353H

TABLE 7: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Word-Program	555H	AAH	2AAH	55H	555H	A0H	WA[3]	Data				
Sector-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA_X[4]	50H
Block-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA_X[4]	30H
Chip-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Erase-Suspend	XXXH	B0H										
Erase-Resume	XXXH	30H										
Query Sec ID[5]	555H	AAH	2AAH	55H	555H	88H						
User Security ID Word-Program	555H	AAH	2AAH	55H	555H	A5H	SIWA[6]	Data				
User Security ID Program Lock-out	555H	AAH	2AAH	55H	555H	85H	XXXH	0000H				
Software ID Entry[7,8]	555H	AAH	2AAH	55H	BK_X[4] 555H	90H						
CFI Query Entry[8]	555H	AAH	2AAH	55H	BK_X[4] 555H	98H						
CFI Query Entry[8]	BK_X[4] 55H	98H										
Software ID Exit/ CFI Exit/ Sec ID Exit[9,10]	555H	AAH	2AAH	55H	555H	F0H						
Software ID Exit/ CFI Exit/ Sec ID Exit[9,10]	XXH	F0H										

T7.0 1270

1. Address format A_{10}-A_0 (Hex), Addresses A_{20}-A_{11} can be V_{IL} or V_{IH}, but no other value (unless otherwise stated), for the command sequence when in x16 mode.
   When in x8 mode, Addresses A_{20}-A_{12}, Address A_{-1}, and DQ_{14}-DQ_8 can be V_{IL} or V_{IH}, but no other value (unless otherwise stated), for the command sequence.
2. DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for the command sequence
3. WA = Program word address
4. SA_X for Sector-Erase; uses A_{20}-A_{11} address lines
   BA_X for Block-Erase; uses A_{20}-A_{15} address lines
   BK_X for Bank Address; uses A_{20}-A_{18} address lines
5. For SST36VF3203 the Security ID Address Range is: (x16 mode) = 10000H to 100087H,(x8 mode) = 100000H to 10010FH
   SST ID is read at Address Range(x16 mode) = 100000H to 100007H (x8 mode) = 100000H to 10000FH
   User ID is read at Address Range(x16 mode) = 100008H to 100087H (x8 mode) = 100010H to 10010FH
   Lock status is read at Address 0000FFH (x16) or 0001FFH (x8). Unlocked: DQ3 = 1 / Locked: DQ3 = 0.
   For SST36VF3204 the Security ID Address Range is:(x16 mode) = 0FF000H to 0FF087H, (x8 mode) = 000000H to 00010FH
   SST ID is read at Address Range (x16 mode) = 000000H to 000007H (x8 mode) = 000000H to 0000FFH
   User ID is read at Address Range (x16 mode) = 000008H to 000087H (x8 mode) = 000100H to 00010FH
   Lock Status is read at Address 0000FFH (x16) or 0001FFH (x8). Unlocked: DQ3 = 1 / Locked: DQ3 = 0
6. SIWA = Valid Word addresses for user Sec ID
   For SST36VF3203 User ID valid Address Range is (x16 mode) = 100008H-100087H (x8 mode) = 100010H-10010FH.
   For SST36VF3204 User ID valid Address Range is (x16 mode) = 000008H-000087H (x8 mode) = 000010H-00010FH.
   All 4 cycles of User Security ID Program and Program Lock-out must be completed before going back to Read-Array mode.
7. The device does not remain in Software Product Identification mode if powered down.
8. A_{20}, A_{19} and A_{18} = BK_X (Bank Address): address of the bank that is switched to Software ID/CFI Mode
   With A_{17}-A_1 = 0;SST Manufacturer's ID = 00BFH, is read with A_0 = 0
   SST36VF3203 Device ID = 7354H, is read with A_0 = 1
   SST36VF3204 Device ID = 7353H, is read with A_0 = 1
9. Both Software ID Exit operations are equivalent
10. If users never lock after programming, User Sec ID can be programmed over the previously unprogrammed bits (data=1) using the User Sec ID mode again (the programmed "0" bits cannot be reversed to "1").

TABLE 8: CFI QUERY IDENTIFICATION STRING[1]

Address x16 Mode	Address x8 Mode	Data[2]	Description
10H	20H	0051H	Query Unique ASCII string “QRY”
11H	22H	0052H	
12H	24H	0059H	
13H	26H	0001H	Primary OEM command set
14H	28H	0007H	
15H	2AH	0000H	Address for Primary Extended Table
16H	2CH	0000H	
17H	2EH	0000H	Alternate OEM command set (00H = none exists)
18H	30H	0000H	
19H	32H	0000H	Address for Alternate OEM extended Table (00H = none exits)
1AH	34H	0000H	

T8.0 1270

1. Refer to CFI publication 100 for more details.
2. In x8 mode, only the lower byte of data is output.

TABLE 9: SYSTEM INTERFACE INFORMATION

Address x16 Mode	Address x8 Mode	Data[1]	Description
1BH	36H	0027H	V_{DD} Min (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1CH	38H	0036H	V_{DD} Max (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1DH	3AH	0000H	V_{PP} min (00H = no V_{PP} pin)
1EH	3CH	0000H	V_{PP} max (00H = no V_{PP} pin)
1FH	3EH	0004H	Typical time out for Program 2^N µs (2^4 = 16 µs)
20H	40H	0000H	Typical time out for min size buffer program 2^N µs (00H = not supported)
21H	42H	0004H	Typical time out for individual Sector/Block-Erase 2^N ms (2^4 = 16 ms)
22H	44H	0006H	Typical time out for Chip-Erase 2^N ms (2^6 = 64 ms)
23H	46H	0001H	Maximum time out for Program 2^N times typical (2^1 x 2^4 = 32 µs)
24H	48H	0000H	Maximum time out for buffer program 2^N times typical
25H	4AH	0001H	Maximum time out for individual Sector-/Block-Erase 2^N times typical (2^1 x 2^4 = 32 ms)
26H	4CH	0001H	Maximum time out for Chip-Erase 2^N times typical (2^1 x 2^6 = 128 ms)

T9.0 1270

1. In x8 mode, only the lower byte of data is output.

TABLE 10: DEVICE GEOMETRY INFORMATION

Address x16 Mode	Address x8 Mode	Data[1]	Description
27H	4EH	0016H	Device size = 2^N Bytes (16H = 22; 2^{22} = 4 MByte)
28H	50H	0002H	Flash Device Interface description; 0002H = x8/x16 asynchronous interface
29H	52H	0000H	
2AH	54H	0000H	Maximum number of bytes in multi-byte write = 2^N (00H = not supported)
2BH	56H	0000H	
2CH	58H	0002H	Number of Erase Sector/Block sizes supported by device
2DH	5AH	00FFH	Sector Information (y + 1 = Number of sectors; z x 256B = sector size)
2EH	5CH	0003H	y = 1023 + 1 = 1024 sectors (03FFH = 1023)
2FH	5EH	0010H	
30H	60H	0000H	z = 16 x 256 Bytes = 4 KByte/sector (0010H = 16)
31H	62H	003FH	Block Information (y + 1 = Number of blocks; z x 256B = block size)
32H	64H	0000H	y = 63 + 1 = 64 blocks (003FH = 63)
33H	66H	0000H	
34H	68H	0001H	z = 256 x 256 Bytes = 64 KByte/block (0100H = 256)

T10.1 1270

1. In x8 mode, only the lower byte of data is output.

Advance Information

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature[1] . . . . . 260°C for 10 seconds
Output Short Circuit Current . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF
See Figures 17 and 18	

TABLE 11: DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.6V

Symbol	Parameter	Freq	Limits			Test Conditions
			Min	Max	Units	
I_{DD}[1]	Active V_{DD} Current					
	Read	5 MHz		15	mA	CE#=V_{IL}, WE#=OE#=V_{IH}
		1 MHz		4	mA	
	Program and Erase			30	mA	CE#=WE#=V_{IL}, OE#=V_{IH}
	Concurrent Read/Write	5 MHz		45	mA	CE#=V_{IL}, OE#=V_{IH}
		1 MHz		35	mA	
I_{SB}	Standby V_{DD} Current			20	µA	CE#, RST#=V_{DD}±0.3V
I_{ALP}	Auto Low Power V_{DD} Current			20	µA	CE#=0.1V, V_{DD}=V_{DD} Max WE#=V_{DD}-0.1V Address inputs=0.1V or V_{DD}-0.1V
I_{RT}	Reset V_{DD} Current			20	µA	RST#=GND
I_{LI}	Input Leakage Current			1	µA	V_{IN} =GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LIW}	Input Leakage Current on WP# pin and RST# pin			10	µA	WP#=GND to V_{DD}, V_{DD}=V_{DD} Max RST#=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current			1	µA	V_{OUT} =GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage			0.8	V	V_{DD}=V_{DD} Min
V_{ILC}	Input Low Voltage (CMOS)			0.3	V	V_{DD}=V_{DD} Max
V_{IH}	Input High Voltage		0.7 V_{DD}	V_{DD}+0.3	V	V_{DD}=V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)		V_{DD}-0.3	V_{DD}+0.3	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage			0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage		V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

T11.1 1270

1. Address input = V_{ILT}/V_{IHT}, V_{DD}=V_{DD} Max (See Figure 17)

TABLE 12: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T12.0 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13: CAPACITANCE (T_A = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	10 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10 pF

T13.0 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 14: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T14.0 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 15: READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.6V

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	70		ns
T_{CE}	Chip Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		30	ns
T_{CLZ}[1]	CE# Low to Active Output	0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		ns
T_{CHZ}[1]	CE# High to High-Z Output		16	ns
T_{OHZ}[1]	OE# High to High-Z Output		16	ns
T_{OH}[1]	Output Hold from Address Change	0		ns
T_{RP}[1]	RST# Pulse Width	500		ns
T_{RHR}[1]	RST# High before Read	50		ns
T_{RY}[1,2]	RST# Pin Low to Read Mode		20	µs

T15.1 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
   This parameter does not apply to Chip-Erase operations.

TABLE 16: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Program Time		10	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms
T_{ES}	Erase-Suspend Latency		20	µs
T_{BY}[1,2]	RY/BY# Delay Time	90		ns
T_{BR}[1]	Bus Recovery Time		0	µs

T16.-0 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
   This parameter does not apply to Chip-Erase operations.

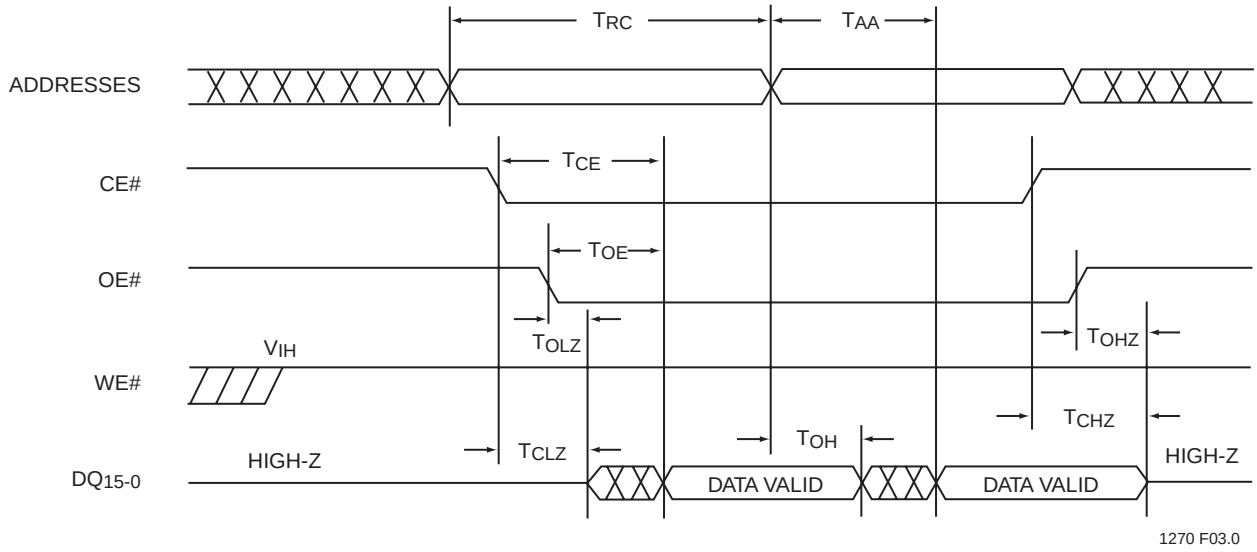
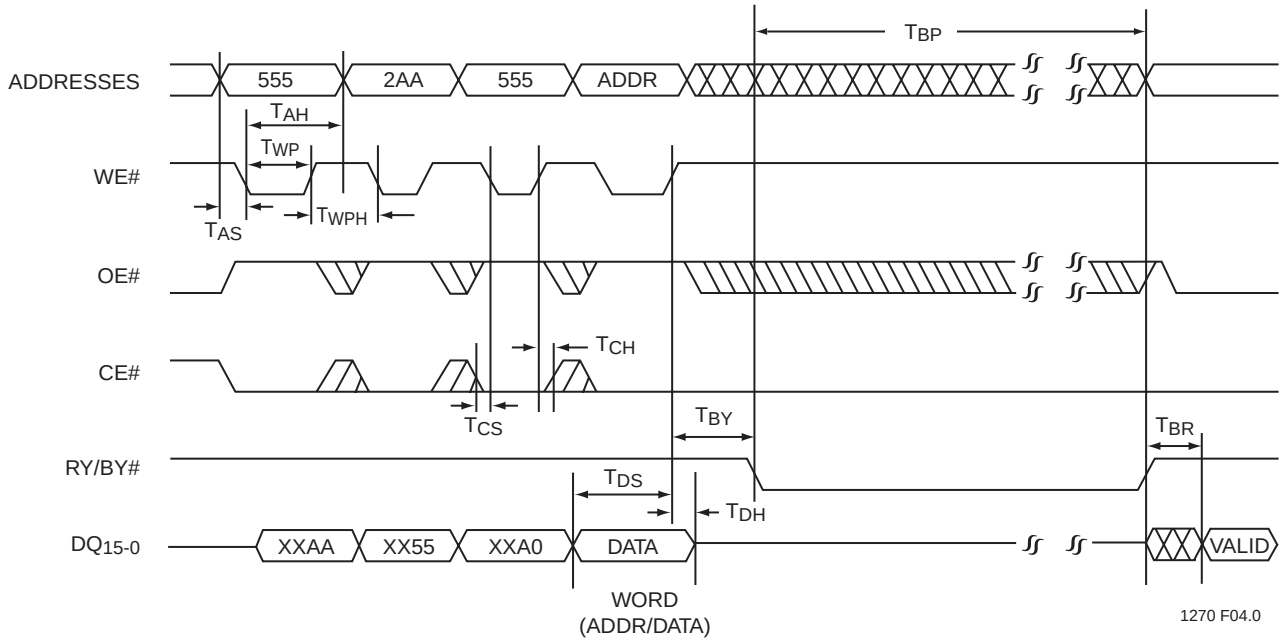
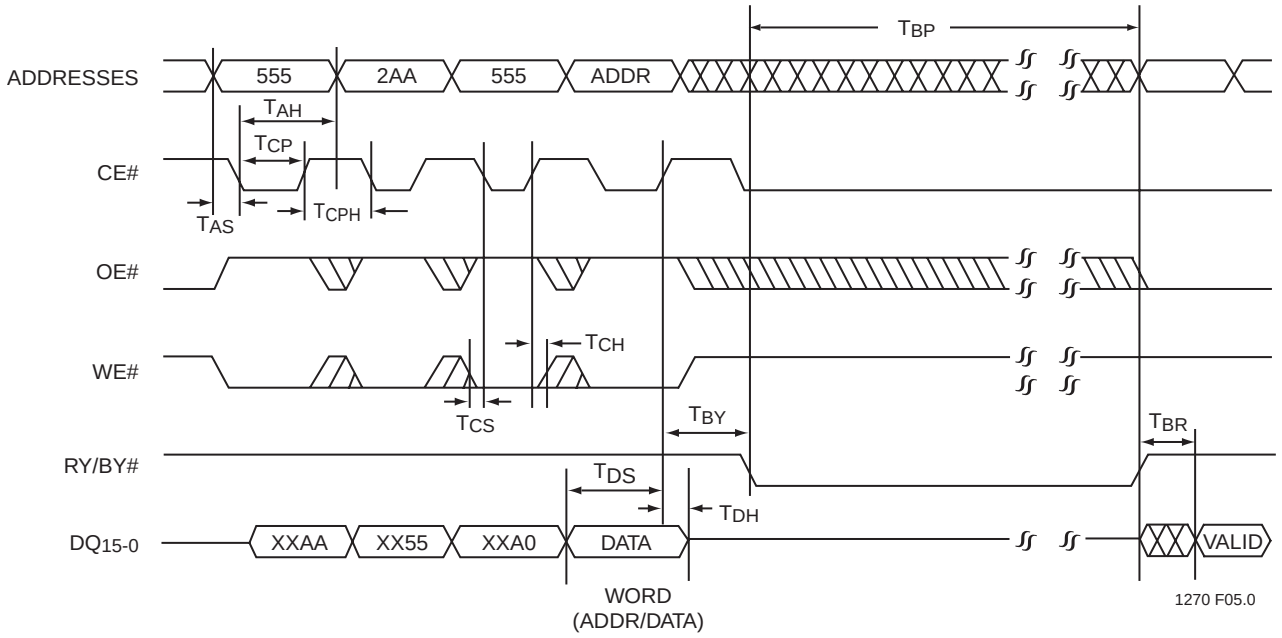


FIGURE 3: READ CYCLE TIMING DIAGRAM



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 4: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 5: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

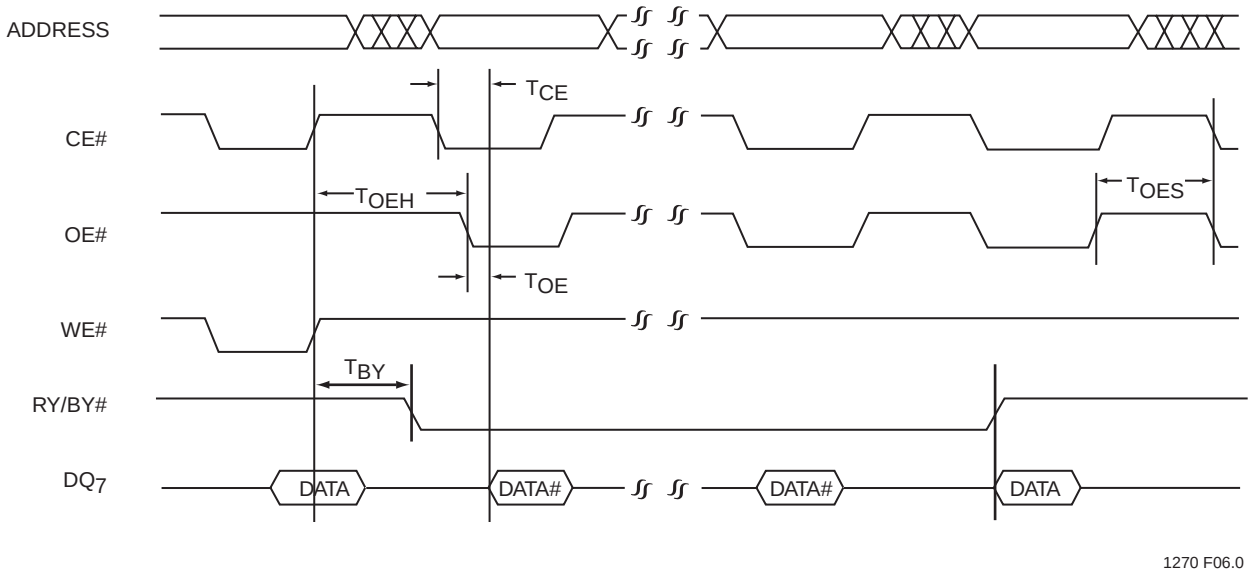


FIGURE 6: DATA# POLLING TIMING DIAGRAM

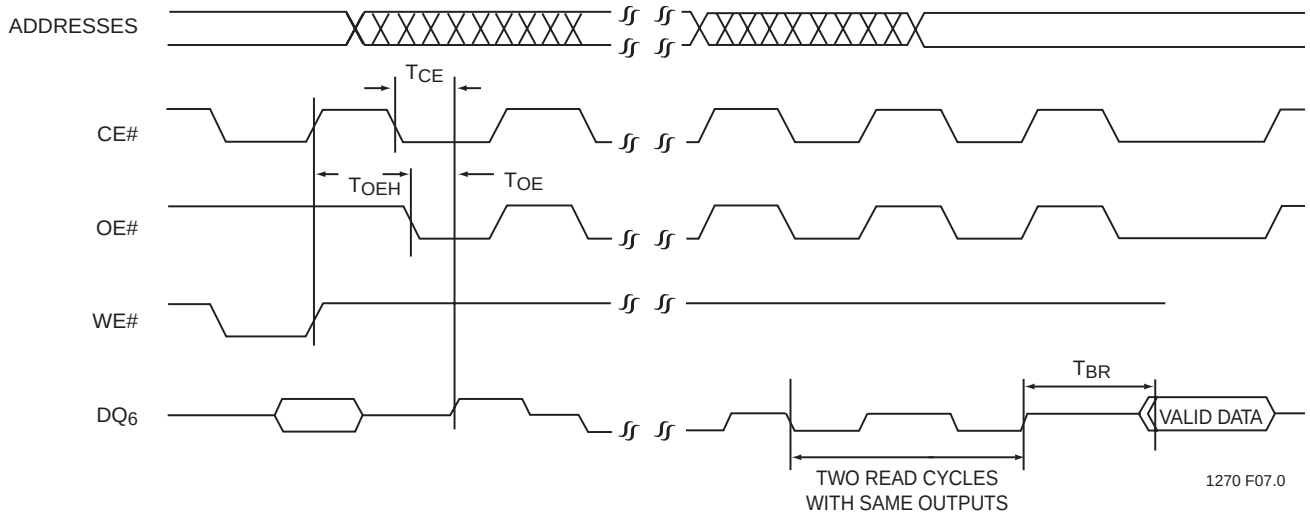
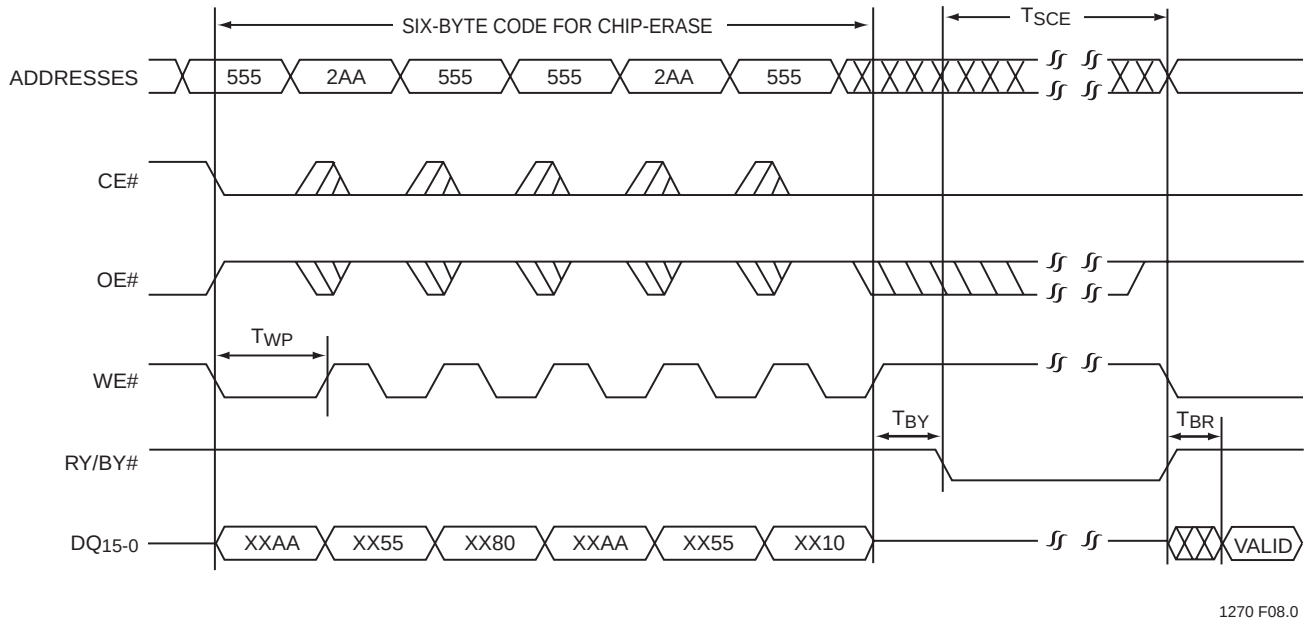
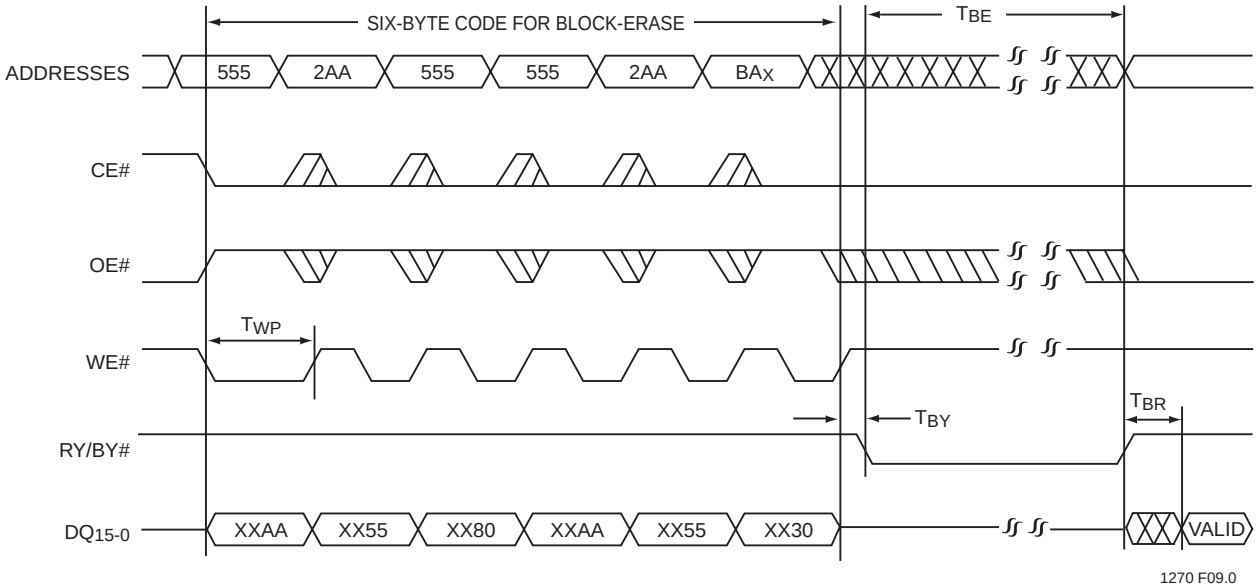


FIGURE 7: TOGGLE BIT TIMING DIAGRAM



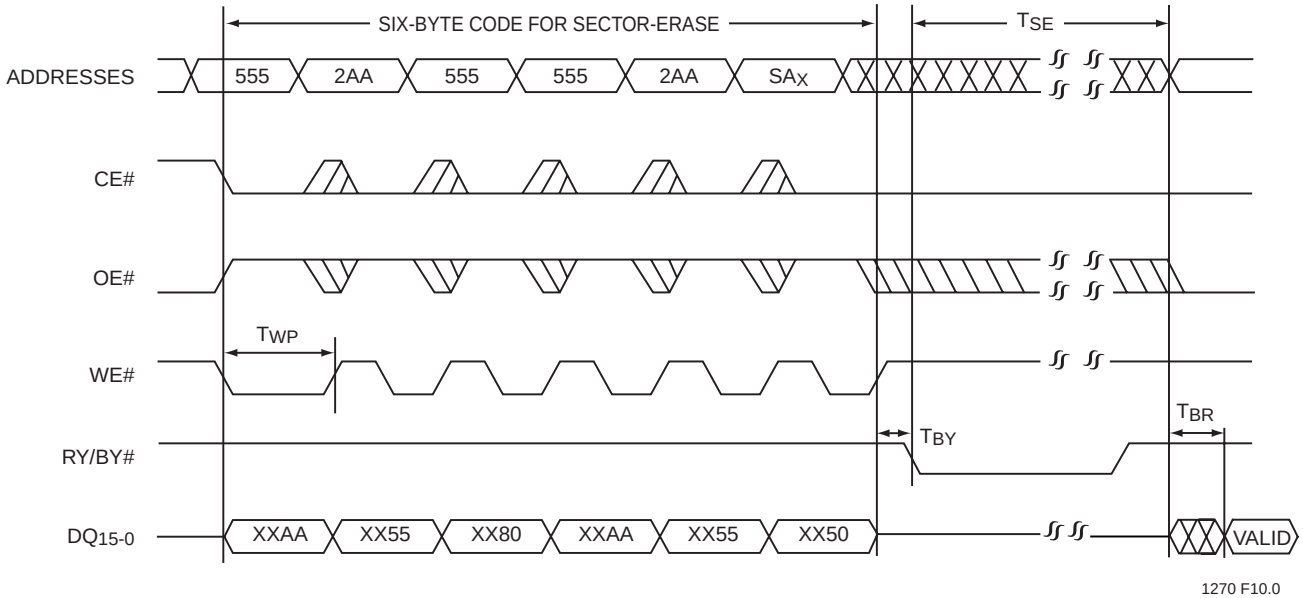
Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 16)
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 8: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



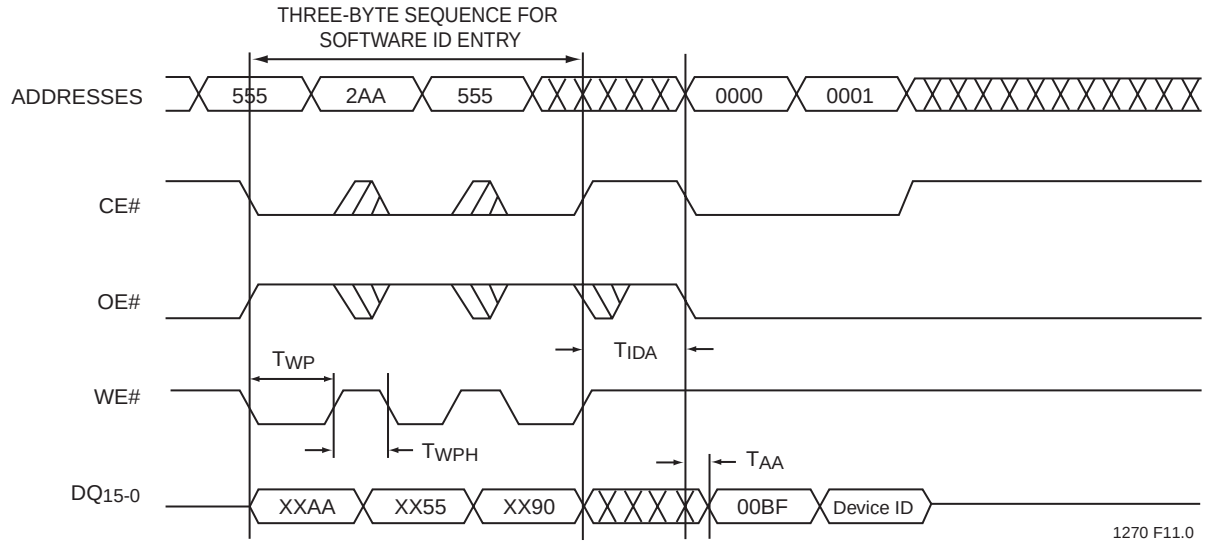
Note: This device also supports CE# controlled Block-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 16)
BA_X = Block Address
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 9: WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM



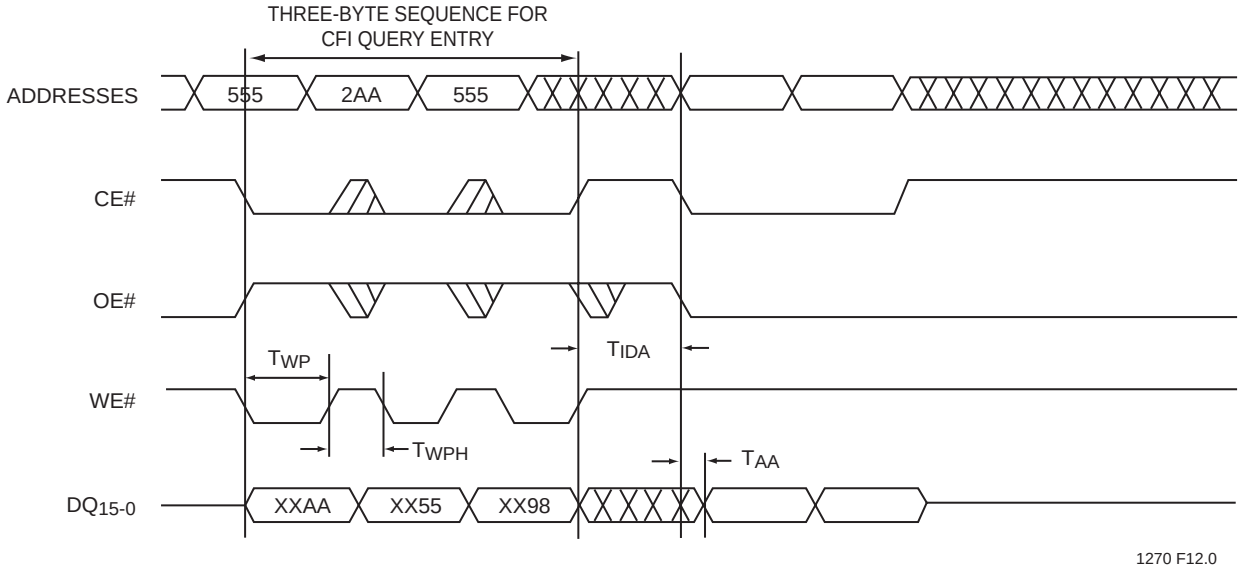
Note: This device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 16)
SA_X = Sector Address
X can be V_{IL} or $V_{IH,}$ but no other value.

FIGURE 10: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



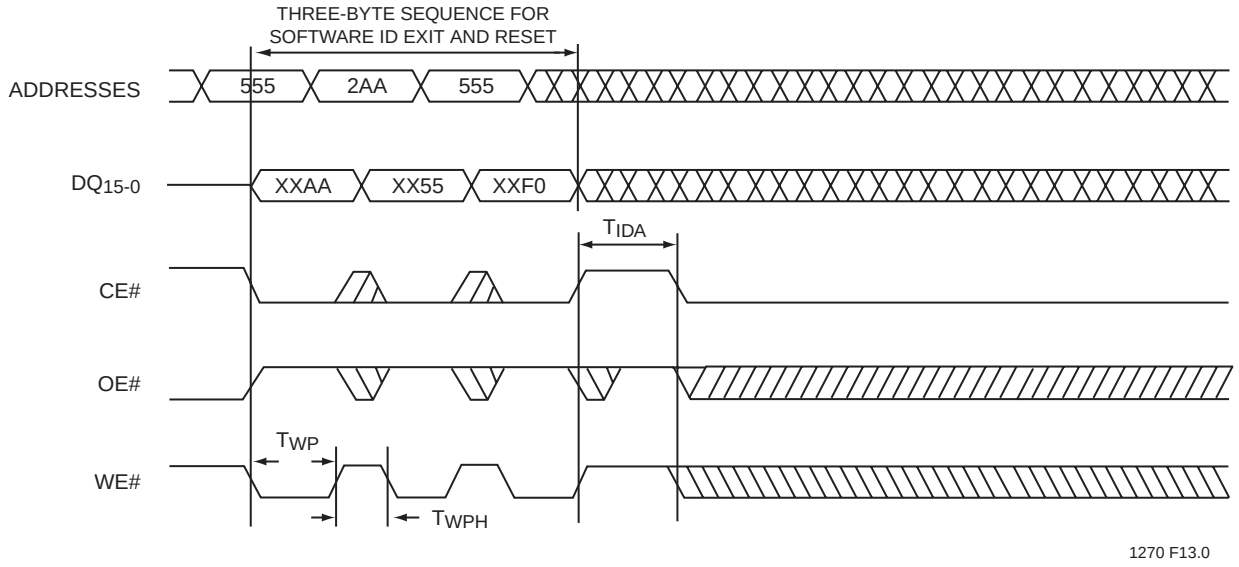
Device ID = 7354H for SST36VF3203 and 7353H for SST36VF3204
Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 11: SOFTWARE ID ENTRY AND READ



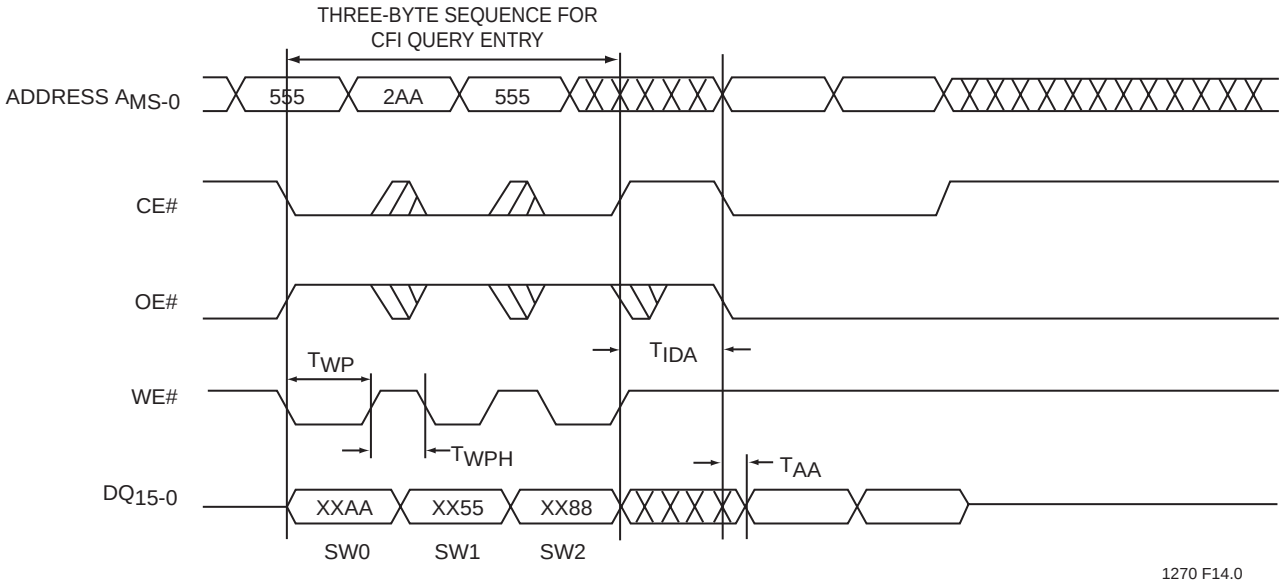
Note: X can be V_{IL} or $V_{IH,}$ but no other value.

FIGURE 12: CFI ENTRY AND READ



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 13: SOFTWARE ID EXIT/CFI EXIT



Note: A_{MS} = Most significant address
$A_{MS} = A_{20}$ for SST39VF3203/3204
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 14: SEC ID ENTRY

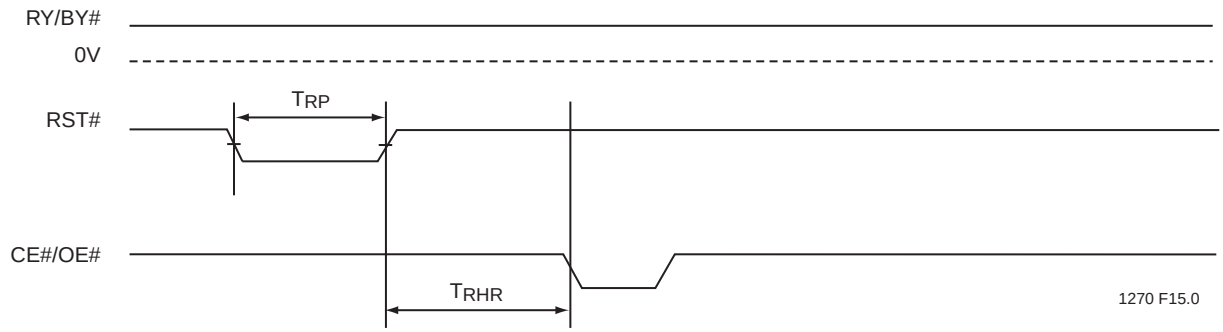


FIGURE 15: RST# TIMING DIAGRAM (WHEN NO INTERNAL OPERATION IS IN PROGRESS)

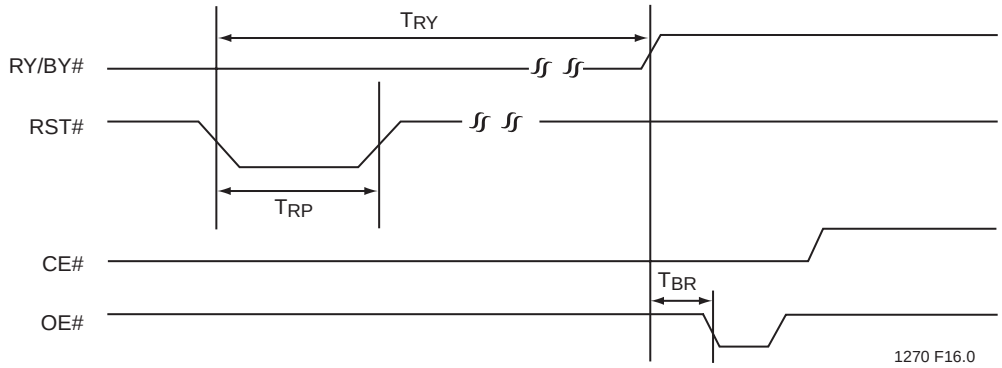
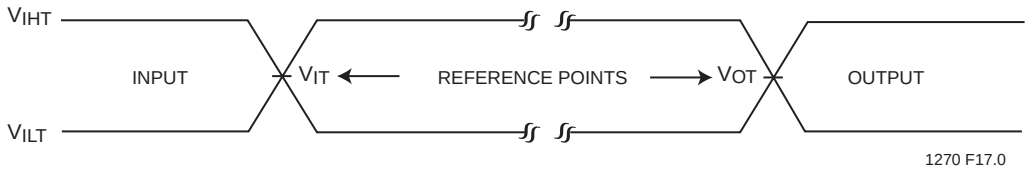


FIGURE 16: RST# TIMING DIAGRAM (DURING SECTOR- OR BLOCK-ERASE OPERATION)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 17: AC INPUT/OUTPUT REFERENCE WAVEFORMS

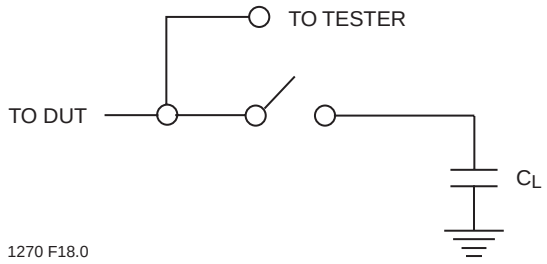
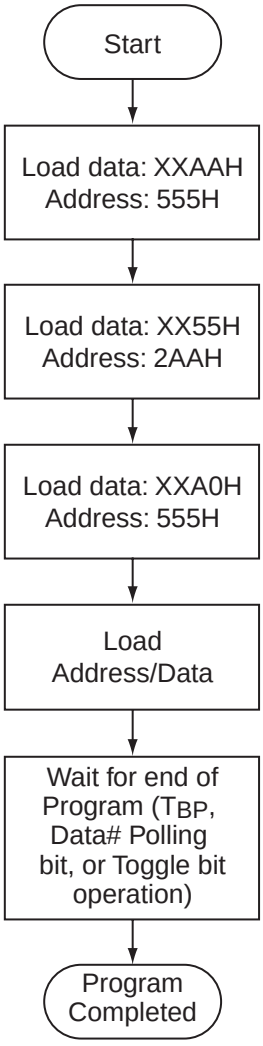


FIGURE 18: A TEST LOAD EXAMPLE



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 19: WORD-PROGRAM ALGORITHM

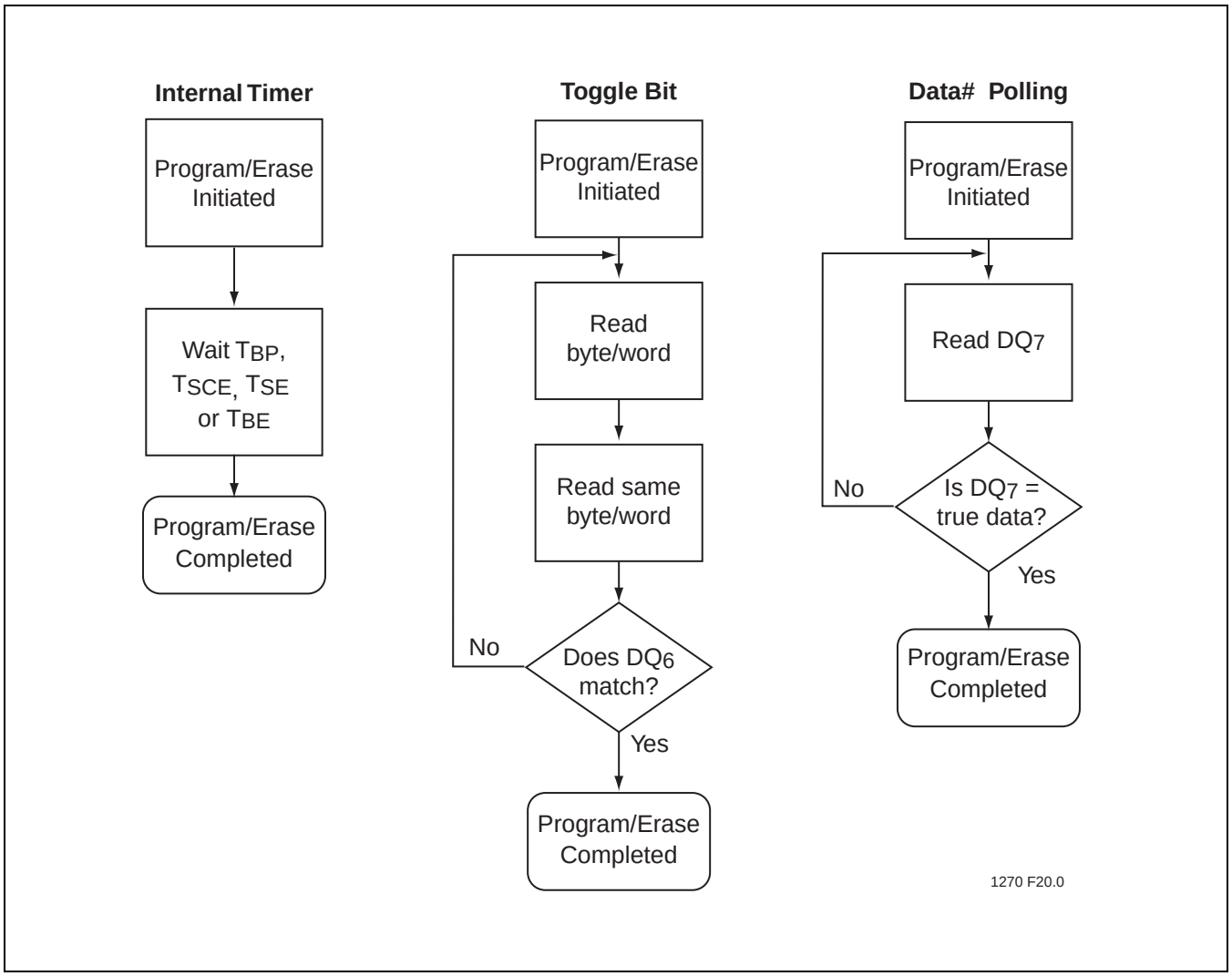


FIGURE 20: WAIT OPTIONS

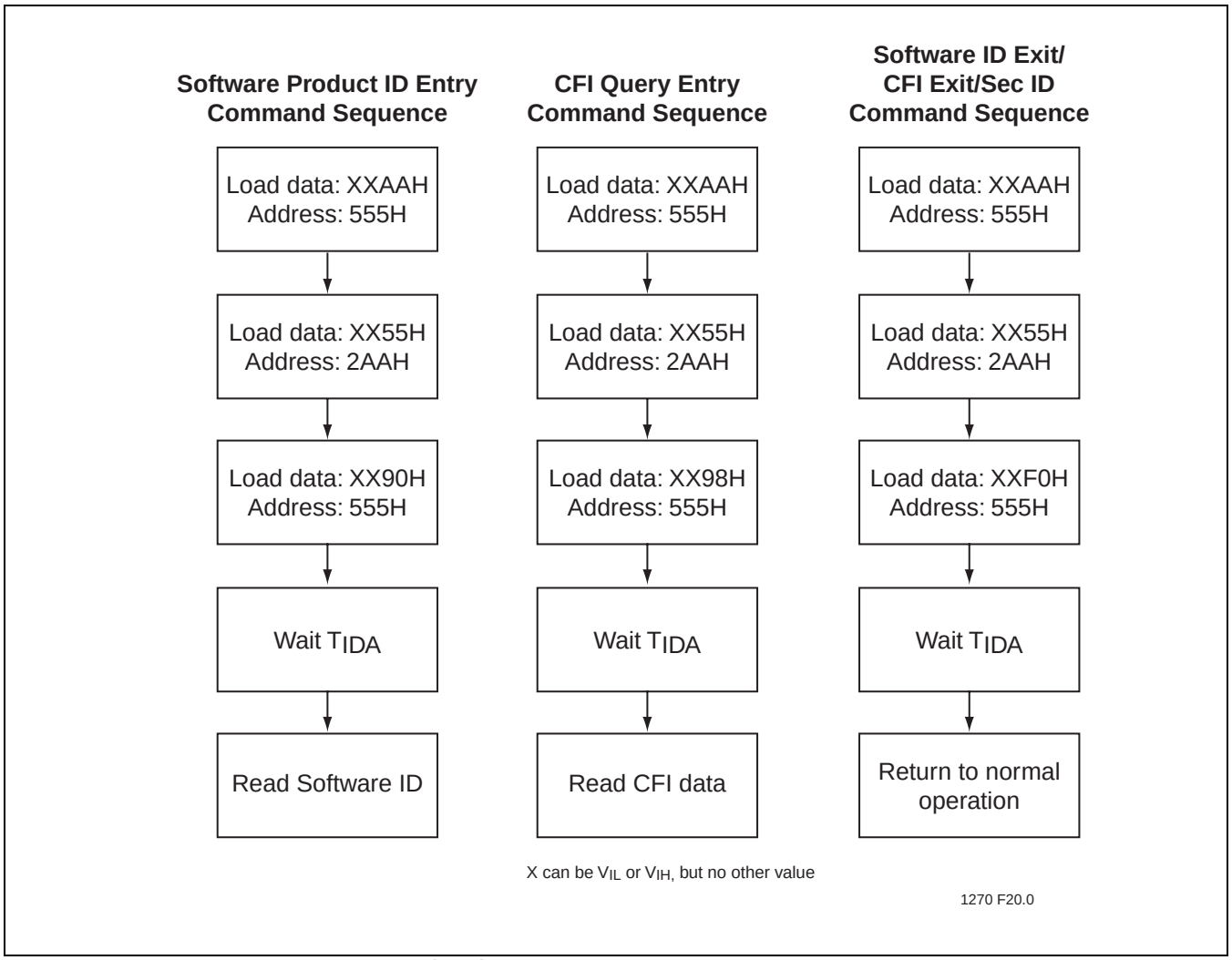
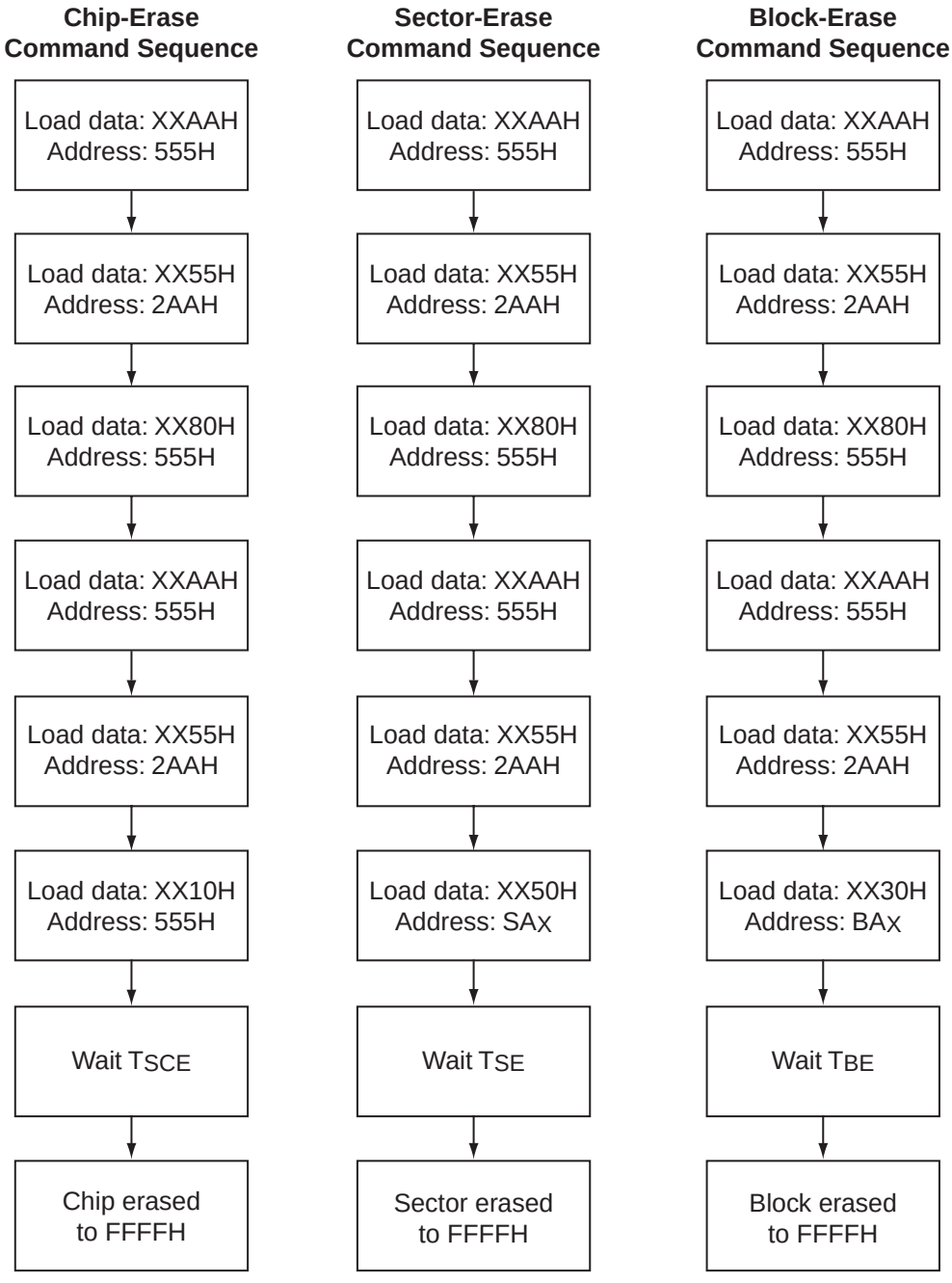


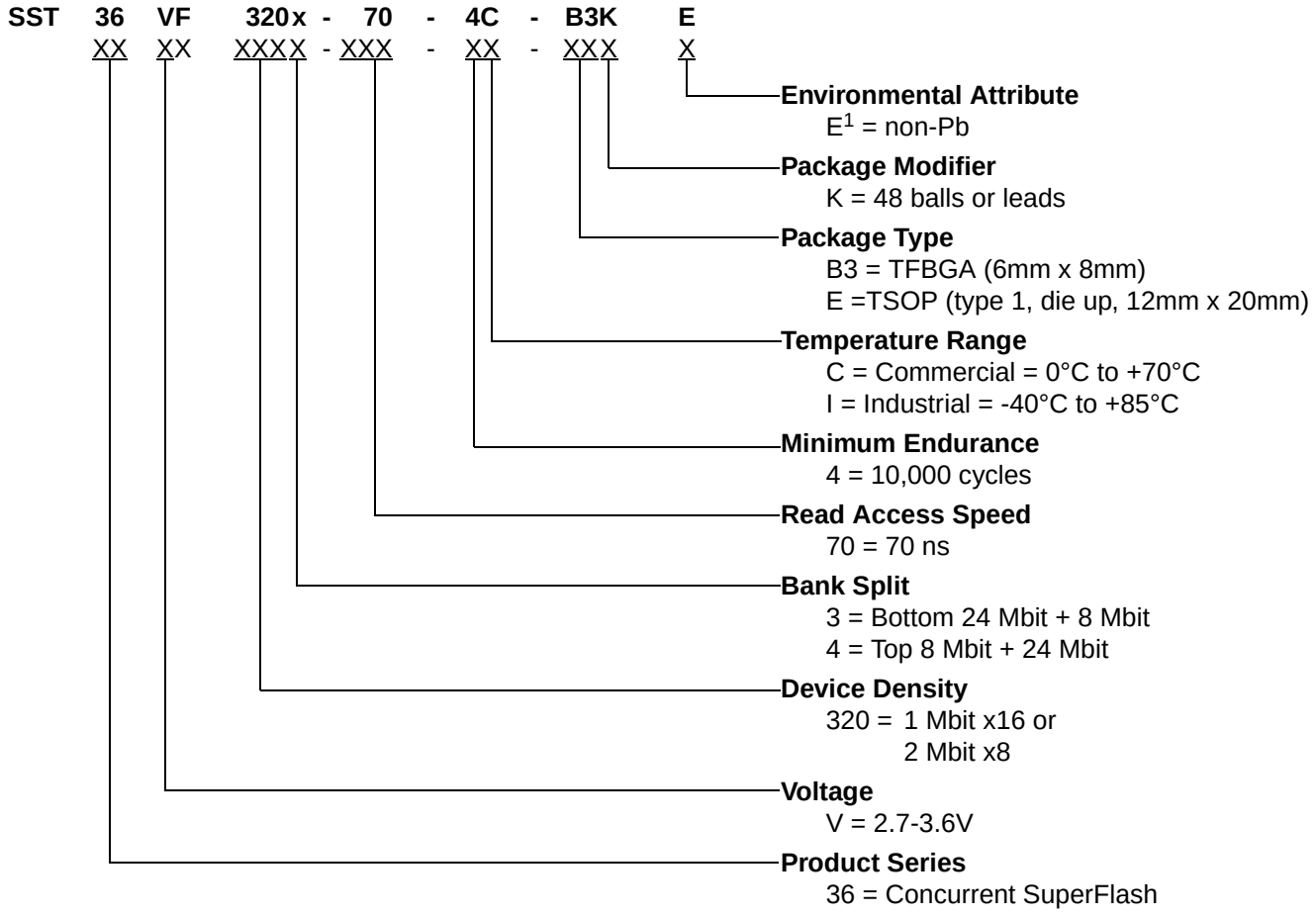
FIGURE 21: SOFTWARE PRODUCT ID/CFI/SEC ID ENTRY COMMAND FLOWCHARTS



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 22: ERASE COMMAND SEQUENCE

PRODUCT ORDERING INFORMATION



1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST36VF3203

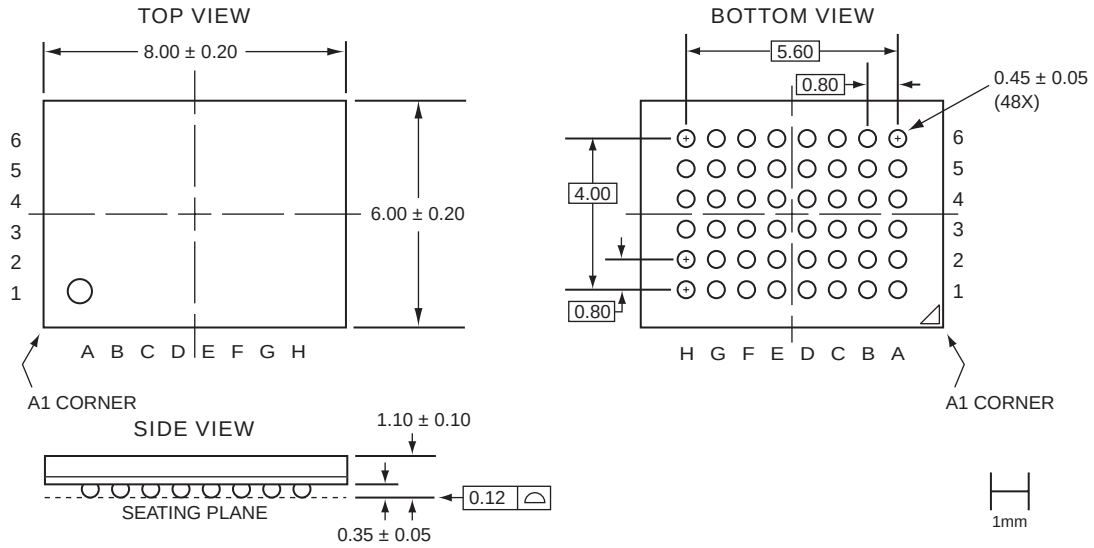
SST36VF3203-70-4C-B3K	SST36VF3203-70-4C-EK
SST36VF3203-70-4C-B3KE	SST36VF3203-70-4C-EKE
SST36VF3203-70-4I-B3K	SST36VF3203-70-4I-EK
SST36VF3203-70-4I-B3KE	SST36VF3203-70-4I-EKE

Valid combinations for SST36VF3204

SST36VF3204-70-4C-B3K	SST36VF3204-70-4C-EK
SST36VF3204-70-4C-B3KE	SST36VF3204-70-4C-EKE
SST36VF3204-70-4I-B3K	SST36VF3204-70-4I-EK
SST36VF3204-70-4I-B3KE	SST36VF3204-70-4I-EKE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

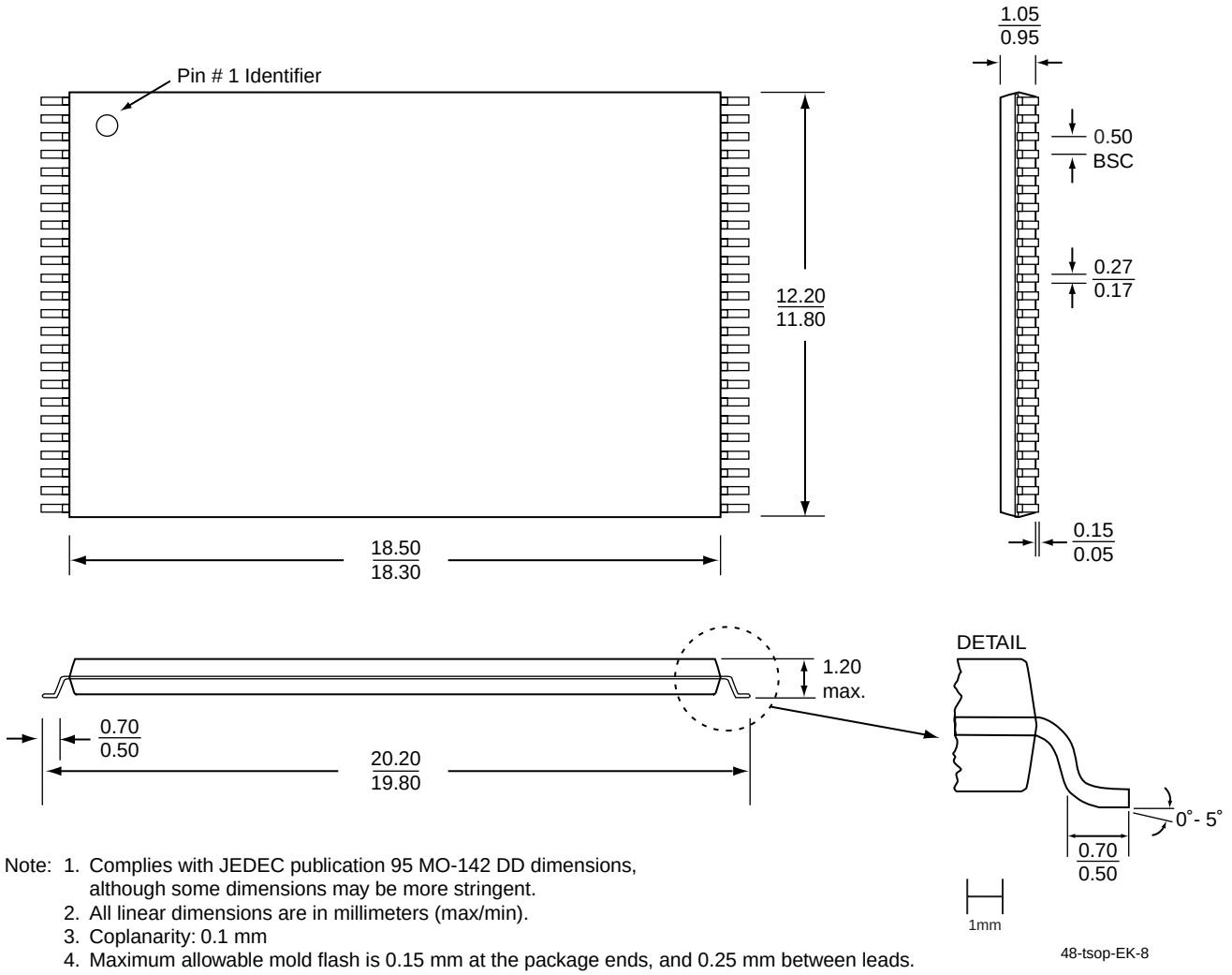
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC Publication 95, MO-210, variant 'AB-1', although some dimensions may be more stringent.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (± 0.05 mm)

48-tfbga-B3K-6x8-450mic-4

48-BALL THIN-PROFILE, FINE-PITCH BALL GRID ARRAY (TFBGA) 6MM X 8MM
SST PACKAGE CODE: B3K



Note: 1. Complies with JEDEC publication 95 MO-142 DD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

48-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 12MM X 20MM
SST PACKAGE CODE: EK

TABLE 17: REVISION HISTORY

Number	Description	Date
00	• Initial release of data sheet	Feb 2005